Seminar Schedule - Monday 16 September

Time	Track A	Track B	Track C
Room	Utopia A	Utopia B	Utopia C
8:00 AM – 12:00 PM	ATE from A to Z	Design for Built-In (Self) Test	ATS Considerations for New Testing Technologies
1:00 PM – 5:00 PM	ATE & TPS Management	Diagnostic Modeling and Application Development	VXI, PXI, IVI, LXI and AXIe Standards Improve ATE Systems Design

TECHNICAL SEMINARS

Monday, 16 September, 2013

AUTOTESTCON seminar attendees receive Continuing Education Unit (CEU) credits. The seminar program has been approved to award CEUs to eligible participants. Qualifying attendees will receive 0.4 CEUs for each successfully completed seminar and 0.8 CEUs for participating in a full day. CEUs can be converted to Professional Development Hours (PDH) required by many states to maintain a professional engineering license. A full day of successful attendance will provide 8 PDH units. CEUs are awarded through the International Association for Continuing Education and Training. The Institute of Electrical and Electronic Engineers, Inc. (IEEE) is an Authorized CEU Sponsor Member of the International Association of Continuing Education and Training.

ATE from A to Z

Track A: 8:00 AM - 12:00 PM
Room: Utopia A

Instructor: Mike Ellis, Northrop Grumman Corporation

This seminar provides a complete overview of the world of ATE from a practical engineering and management viewpoint. Beginning by examining the ATE interfaces and their limitations, it offers managers and project engineers a quick and purposeful insight into the probable sources and causes of potential technical and management problems. Working from the interfaces, the seminar explores analog and digital test methods, examines the impact of new instrument technologies and covers the basics of switching systems and pin electronics.

The seminar will explore the elements of ATE SW, examining the role of each and the scaled limitations that they impose at the s level. ATE languages will also be discussed and the different language types analyzed to determine their effect on ATE and TPS performance.

Software now makes up over 50% of almost all military systems so no discussion of Automated Testing would be complete without exploring the need to consider SW testing as an integral part of the ATS environment. The seminar will discuss the impact of the growth in SW, look at some catastrophic examples of what happens when we inadequately test software and discuss test requirements and methods.

The seminar will conclude with a discussion of recent changes in DoD acquisition strategies and their potential impact on the future of ATE. Interoperability, net-centric operations, nanotechnology and smart sensors are high on OSD’s wish-list for new systems and will become an inherent part of the test and maintenance process. Explore DoD’s vision of the next generation of systems, where Test & Evaluation, Condition Based Maintenance, Training and Battle Damage Assessment become by-products of a distributed hierarchical, real-time information network. The future may be closer than you think!

TECHNICAL SEMINARS

ATE & TPS Management

Track A: 1:00 PM - 5:00 PM
Room: Utopia A

Instructor: Mike Ellis, Northrop Grumman Corporation

This four-part seminar is designed to cover the controversial and challenging issues of managing ATE and TPS development. This session is a must for all industry and government ATE/TPS managers. As with the morning ATE session, it focuses on real world situations and explores areas of frequent problems.

Part 1: This section of the Seminar covers the tasks and challenges facing the government Acquisition Manager in preparing for, awarding and oversight of a TPS acquisition contract. It is based on the NAVAIR Generic OTPS RFP (aka Red Team) chaired by Ed Holland (NAVAIR retired). The session will cover the issues faced by the military in acquiring TPSs, but the general acquisition strategy is also common to ATE acquisitions.

Part 2: This portion of the seminar deals with the challenges facing the TPS Developer. It summarizes the lessons learned from 20 years of TPS Development Management on over 1000 TPSs for all armed service branches. This part of the seminar will focus on planning and controlling a military TPS development project. Planning objectives will be those elusive goals, happy customer and a profitable project.

Part 3: TPS Seminar attendees will be provided in-depth insight into actual issues faced during TPS Acceptance Testing. This seminar section will lead attendees through an actual Acceptance Test, highlighting and discussing real-world problems and their resolution from the viewpoint of buyer and seller. Parts 2 and 3 will be taught by Mike Ellis of Northrop Grumman Corporation, and will draw upon over two decades of ATE and TPS consulting experience.

Part 4: No ATE seminar would be complete without a discussion of commercial-off-the-shelf (COTS) hardware and software. A to Z will include a realistic, and entertaining examination of (COTS) application to the military ATE environment. Initially viewed as a panacea, it is now recognized that despite its many advantages, COTS is not a “free lunch". Attendees are invited to visit “The Underside of the COTS Iceberg,” where they will travel through an actual COTS rehost of a complex ATE system. Take this opportunity to explore both sides of the COTS revolution, understanding both its opportunities and its challenges, while examining and learning from “other people’s mistakes.”

This unique four-part seminar offers attendees the opportunity to "live" each of the TPS life cycle phases through the eyes of experts. Along the way attendees will have the opportunity to examine the product and its challenges from four distinctly different viewpoints. They will explore the "pot holes" in the path to success and have the opportunity to understand the implementation and impact associated with effective, on-time TPSs delivered within budget.

Design for Built-In (Self) Test

Track B: 8:00 AM - 12:00 PM
Room: Utopia B

Instructor: Louis Y. Ungar, A.T.E. Solutions, Inc.

With increased circuit complexity in recent years *almost* every test approach has had to settle for lower fault coverage, more difficulty in diagnoses and all at greater costs. The notable exception is Built-In Test (or Built-in Self-Test, BIST) or as it is often called, embedded test. BIST is a phenomenon that capitalizes on greater circuit complexity (intelligence), better fault isolation from a hierarchical allocation of tests, and does not rely on costly external automatic test equipment (ATE) and test program sets (TPS). The inclusion of boundary-scan circuitry in increasing numbers of today's chips has made circuit testability more readily available at board and system levels. Inclusion of BIST structures in less, but significant number of chips, has made it possible to invoke chip-level tests even during normal operation. These two developments, already in place for the past several years, and greatly accelerated in the past few years, have not only made component-level, board-level and system-level BIST possible to run after system deployment, but it has also made hierarchical BIST feasible. With hierarchical BIST, diagnostic resolutions can be greatly improved, and self-testing, self-diagnostic, even self-prognostic systems are achievable.

This seminar is aimed at professionals in all areas of support, including reliability, maintainability and logistics, as well as engineers and managers from design, test, and quality assurance.

The course will discuss how test issues can be effectively dealt with at the design level by creating testable circuits. Using boundary scan (JTAG/IEEE-1149.1) techniques, as well as mixed signal (IEEE-1149.4) and AC-coupled nets (IEEE-1149.6) testability standards, it is now possible to gain chip-level access through a system-level connector. Combining these techniques with internal scan and BIST structures, attendees will learn how to design tests into a circuit. Utilizing BIST structures that are increasingly embedded into chips, or programmed into field programmable gate arrays (FPGAs) through JTAG in-system programming (ISP), a larger percentage of the circuit can be made testable. The cost of using such techniques is on the decline, while the benefits that can be gained are ever greater. While software approaches to built-in test are mature and widely accepted at the system-level, project managers need to consider the added rewards of hardware BIST. It can improve diagnostics, reduce the expense of ATE and of test program set (TPS) development, and offer a platform for prognoses. In some circuits, such as memories, BIST gives way to built-in repair analysis, and even built-in self-repair.

This course will provide attendees with the understanding they need to plan system designs for test and for built-in tests. The course will also discuss how these techniques affect supportability issues, including reliability, availability, operational readiness and false alarms.

Diagnostic Modeling and Application Development

Track B: 1:00 PM - 5:00 PM
Room: Utopia B

Instructors: Dr. John W. Sheppard, Montana State University; Timothy J. Wilmering, Boeing

This seminar provides an overview of traditional and more recent approaches to system-level diagnosis and prognosis. The emphasis is placed on different system modeling approaches and the algorithms that can be applied using resulting models. The seminar is organized in three parts:

Part 1: The Diagnostic Landscape. The seminar will begin by reviewing the basic issues and challenges in system diagnosis and prognosis. Fundamental terms and concepts of fault diagnosis will be presented with focus being given to historical approaches and the needs from the perspectives of the Department of Defense. Recent initiatives such as DoD ATS Framework, NxTest, ARGCS, and ATML will also be introduced.

Part 2: Diagnostic and Prognostic Algorithms. In the second part of the seminar, diagnosis will be defined within the context of classification problems. Central to this part of the seminar will be a continuing discussion of how one handles uncertainty in the diagnostic and prognostic process; therefore, the primary focus of this part will be recent developments in applying Bayesian techniques to fault diagnosis and prognosis. Prognosis will be related to the diagnosis problem in the context of “predictive” classification, and Bayesian extensions, such as hidden Markov models and dynamic Bayesian networks will be discussed.

Part 3: Health Management Information Integration. The third part of the seminar will focus on information integration issues in developing health management systems. The discussion will focus on using formal models, called ontologies, to define the semantics of the required information and then focus on processes for maturing diagnostic applications as maintenance information is collected. Emerging standards being developed within the IEEE related to diagnostic and maintenance information will be reviewed. The seminar will end by reviewing the state of the art and providing an overall assessment of how well diagnosis and prognosis can be performed.

Throughout the discussion, the seminar will draw upon experiences of the instructors and participants to highlight issues related to diagnostic development within defense and commercial environments.

ATS Considerations for New Testing Technologies

Track C: 8:00 AM - 12:00 PM
Room: Utopia C

Instructor: Larry V. Kirkland WesTest Engineering, Corp. R. Glenn Wright GMA Industries, Inc.

This seminar addresses the introduction of new testing technologies into today's automatic test systems (ATS) in an effort to fulfill current and future test requirements for printed circuit boards (PCBs). The increasing gate density of electronic components, combined with new levels of functionality equal to entire system levels of just ten years ago, call for new approaches to testing that stretch the imagination and cry out for new definitions of testing philosophies. An interface is no longer limited to direct connections to card-edge connectors and test points, but comprises the complete geometry of the PCB accessible across the entire spectrum from DC to the terahertz region and beyond without relying simply on physical connections. Sensors used for test can range in scale from centimeters to nanometers, both external and internal to the PCB, and are able to observe electrical, chemical, physical and other phenomena previously not capable of being measured. Sensor data processing and failure event interpretation has entered into a new realm of sophistication and complexity to detect and identify not only PCB components (electrical, electromechanical, mechanical and the PCB itself) that have failed, but are likely to fail in the future. More interestingly, the question of what comprises test requirements may now extend beyond specifically what the UUT is supposed to do and when it does it, given a particular set of stimulus, to how and why it does what it does.

Methods of UUT interrogation and observation of circuit board and component behavior via direct connection, wireless, and passive means are discussed. An overview of existing and advanced sensor technologies relating to functionality, test capabilities and limitations, current state of the art, and cost is provided covering: analog and digital, thermal and infrared, electromagnetic emissions, laser vibrometry, X-ray, terahertz, and gas and materials sensors. Hardware and software issues are also considered, addressing such topics as sensor integration and data fusion, visualizing test processes and analyzing test results, robotics as a means of enhanced UUT access, and integration of new technology into existing legacy ATS.

VXI, PXI, IVI, LXI and AXIe Standards Improve ATE Systems Design

Track C: 1:00 PM - 5:00 PM
Room: Utopia C

Instructor: Bob Helsel, currently managing the following T&M consortia: VXIbus Consortium, PXI Systems Alliance, IVI Foundation, LXI Consortium, and AXIe Consortium.

The VXIbus architecture was introduced 26 years ago, and is currently a well-established architecture used extensively in military, aerospace and commercial applications. However, many test engineers have no personal experience with it, or would like to brush up on its basics, as it will be around for another 10-20 years. We will cover the approval in 2004 of the VXI-1 Rev 3.0 spec, which again doubles the backplane speed to 160MB/s. And we will cover the approval of VXI 4.0 and its improvements in speed and flexibility. VXIplug&play standards are the software equivalent to the VXI hardware specifications, and are the definition to which all VXI drivers are now written. This software standard has formed the bedrock for many other software developments, such as Interchangeable Virtual Instrument (IVI) drivers.

PXI is a newer, more compact, faster hardware standard based on CompactPCI. It applies the same extensions to CPCI that VXI did to VME. This modular instrument standard rapidly gained acceptance and can be viewed as a companion standard to VXI, (or by some as a replacement). This 16-year-old hardware standard will be discussed in detail, as will its expected impact on the market. An update will be provided on Enhanced PXI specifications and their implementation, including Low Power Chassis. PXI Express and PXI MultiComputing will be explained with a review of PXI express products and their potential applications.

The Interchangeable Virtual Instrument (IVI) software standard, which has been extensively revised and expanded, will be covered with the latest information available. The IVI Foundation was founded in 1998 and incorporated in 2001. The purpose of the IVI Foundation is promoting specifications for programming test instruments that simplify interchangeability, provide better performance, and reduce the cost of program development and maintenance. IVI Instrument drivers have been available for about 11 years. New Specifications for Digital Test, Counter/Timer, and Signal Oriented test plus LXI triggering and sync will also be discussed.

The LXI Consortium is 8 years old now, and was formed to standardize the way instruments can be connected and controlled via the Internet in a Local Area Network. Extensions for discovery, triggering and synchronization, browser interface, initialization, and programming are all part of the extensions being considered in this standardization effort. We will introduce the latest release of the LXI Specification as well as the introduction of new LXI compliant products that are now available.

An emerging test and measurement standard called AXIe, AdvancedTCA eXtensions for Instrumentation (http://www.axiestandard.org/), is expected to find wide acceptance within the Automatic Test Equipment community as it offers many key benefits. It is expected that a large number of COTS (commercial off-the-shelf) signal conditioning, acquisition and processing modules will become available from a range of different suppliers. AXIe uses AdvancedTCA® as its base standard, but then leverages test and measurement industry standards such as PXI (http://www.pxisa.org/), IVI (http://www.ivifoundation.org/), and LXI (http://www.lxistandard.org/), which were designed to facilitate cooperation and plug-and-play interoperability between COTS instrument suppliers. This enables AXIe systems to easily integrate with other test and measurement equipment. AXIe's large board footprint, available power and efficient cooling to the module payload allows high density in a 19" rack space, enabling the development of high-performance instrumentation in a density unmatched by other instrumentation form factors. Channel synchronization between modules is flexible and provided by AXIe's dual triggering structures: a parallel trigger bus, and radially-distributed, time-matched point-to-point trigger lines. Inter-module communication is also provided with a local bus between adjacent modules allowing data transfer rates up to 10 Gbits/s in each direction, for example between front-end digitizer modules and DSP banks. AXIe is a next-generation, open standard that extends AdvancedTCA® for general purpose and semiconductor test. First specifications were released in June 2010, and a 12-bit, 8 channel AXIe digitizer was elected as the 2013 TM Best in Test winner of the category signal analyzer.

This comprehensive update on the development of commercial standards for the ATE community should not be missed by anyone concerned with current and future ATE systems design and integration.

TECHNICAL SESSIONS SCHEDULE

	TIME	Session	TRACK A	TRACK B	TRACK C
			Schaumburg G	Schaumburg F	Schaumburg E
Tuesday 17-Sep	8:30 AM - 9:45 AM	-	Executive Plenary: Introduction & Keynote (Schaumburg East)		
	2:00 PM - 3:30 PM	1	ATE Systems Design	FPGA Test Applications	Panel: Design for Testability
	3:45 PM - 5:15 PM	2	ATS Management	RF Testing	Panel: Synthetic/Software Defined Instrumentation
Wednesday 18-Sep	8:00 AM - 10:00 AM	3	Executive Plenary Panel (Schaumburg East)		
	10:30 AM - 12:00 PM	4	ATE Techniques & Applications 1	Test Techniques	Panel: Status and Outlook of Modular Instrumentation
	1:30 PM - 3:00 PM	5	ATE Techniques & Applications 2	Test Software Techniques	Panel: Reduce Costs and Future Proof Your Systems Using IVI and LXI Standards
	3:30 PM - 5:00 PM	6	ATE Techniques & Applications 3	Design for Testability	
Thursday 19-Sep	9:00 AM - 10:30 AM	7	ATE Standards	TPS Development	Diagnostics & Prognostics 1
	10:45 AM - 12:15 PM	8	ATE Methods	Test Instrumentation	Diagnostics & Prognostics 2

TECHNICAL SESSIONS

Tuesday, 17 September, 2013

Executive Plenary: Introduction & Keynote Speaker
8:30 AM - 9:45 AM
Room: Schaumburg East

**See page 8 for information*

ATE Systems Design
SESSION A1
2:00 PM - 3:30 PM
Room: Schaumburg G
Session Chair: Larry V. Kirkland (WesTest Engineering, USA)

Design and Manufacturing of Lauch Support Test Set For ARIRANG-3
Young-Yun Kim (Korea Aerospace Research Institute, Korea)
Dong-Chul Chae (Korea Aerospace Research Institute, Korea)
Jong-Yeoun Choi (Korea Aerospace Research Institute, Korea)
Jae-Wook Kwon (Korea Aerospace Research Institute, Korea)

Developing New Automatic Test Equipments (ATE) using Systematic Design Approaches
H. Alper Toku (ASELSAN Inc., Turkey)

Incorporating Optical Test Capabilities into a Depot Test Platform
Lowell Parsons (Marvin Test Solutions, USA)
Michael Dewey (Marvin Test Solutions, USA)

A Modular, Extendible and Reusable Test Configuration for System-Level Manufacturing Tests
Muharrem Tümçakır (ASELSAN Inc., Turkey)
Çınar Yeşil (ASELSAN Inc., Turkey)
Mert Burkay Çöteli (ASELSAN Inc., Turkey)

FPGA Test Applications
SESSION B1
2:00 PM - 3:30 PM
Room: Schaumburg F
Session Chair: Robert Wade Lowdermilk (RADX Systems, USA)

IVI Revisited: Building Next-Generation Test Systems with Open FPGAs while Preserving Software APIs
Ryan Verret (National Instruments, USA)

Development of Dual-channel High-speed Data Acquisition Card Based on PCI Bus
Wang Liu (Harbin Institute of Technology, P.R. China)
Liyan Qiao (Harbin Institute of Technology, P.R. China)
Yunfeng Liu (Harbin Institute of Technology, P.R. China)

Implementation of Programmable Delay Lines on Off-the-Shelf FPGAs
Yu-Yi Chen (National Taiwan University, Taiwan)
Jiun-Lang Huang (National Taiwan University, Taiwan)
Terry Kuo (OpenATE, Taiwan)

Tuesday, 17 September, 2013

Panel: Design for Testability (DFT): Implementing this most cost effective yet least popular test solution

SESSION C1
2:00 PM - 3:30 PM
Room: Schaumburg E
Moderator: Louis Y. Ungar (A.T.E. Solutions, Inc., USA)

We bring together panelists and the audience to explore ways to get testability and built-in test considerations into systems. This is especially important for commercial-off-the-shelf (COTS) based systems. While it only costs a few hundred dollars to replace a COTS subsystem, it can cost orders of magnitude more to correctly isolate the responsible COTS if it is not testable. The audience will share success stories on how they were able to implement DFT. The take away from anecdotal evidence may save your program big bucks!

Panelists:
Craig Stoldt, *Test & Systems Engineering Manager, BAE Systems, USA*

Von C. Campbell, *Platform Components Segment and R&D Manager, Agilent Technologies, USA*

Zafer Savas, *Test Engineering Manager, ASELSAN, Turkey*

Michael T. Ellis, *Product Line Manager, Navigation Systems, Northrop Grumman Corporation, USA*

ATS Management

SESSION A2
3:45 PM - 5:15 PM
Room: Schaumburg G
Session Chair: Tom Sarfi (VTI Instruments, USA)

A holistic approach to reducing the life cycle costs of test
Duane Lowenstein (Agilent Technologies, USA)
Joe LaGrotta (Agilent Technologies, USA)

Avionic Support for the Foreign Military Sales Customer
Randall Marion (Boeing, USA)

Managing Costs Through Test System Manageability
Matt Anderson (National Instruments, USA)
Tom Bradicich (National Instruments, USA)
Byron Radle (National Instruments, USA)

TECHNICAL SESSIONS

Tuesday, 17 September, 2013

RF Testing
SESSION B2
3:45 PM - 5:15 PM
Room: Schaumburg F
Session Chair: Yonet A Eracar (Teradyne, Inc., USA)

Wideband 20 GHz RF Digitizer and Python-based Open Application Framework for Test and Measurement
Nikhil Adnani (ThinkRF Corp, Canada)
Tim Hember (ThinkRF Corp, Canada)
Tarek Helaly (ThinkRF Corp, Canada)
Mohammad Farhan (ThinkRF Corp, Canada)
Ian Ward (ThinkRF Corp, Canada)

Phase Coherent Signal Creation with up to Twelve Channels with High-Performance Multi-Channel Arbitrary Waveform Generator
Michael May (Agilent Technologies, Inc., Germany)

Using RF Recording Techniques to Resolve Interference Problems
David Murray (Agilent Technologies, Inc., USA)

Tuesday, 17 September, 2013

Panel: Synthetic/Software Defined Instrumentation-Are We There Yet?

SESSION C2
3:45 PM - 5:15 PM
Room: Schaumburg E
Moderator: Dr. Michael N. Granieri (National Instruments, USA)

The technology of Synthetic Instrumentation as a subset of Virtual Instrumentation has been undergoing a steadying maturation process over the past decade. From its modest beginning as an emerging technology as an integral part of the DOD NXTest initiative in the early 2000 time frame, it has emerged as the centerpiece modern day paradigm of software defined instrumentation. Today numerous fielded examples exist in both the DOD and commercial marketplace exemplifying both the power and potential of this disruptive technology.

This panel session will focus on the current state of the technology and an assessment by expert panelists on the projected future prognosis for this most promising technology. The moderator will open the session with a brief overview of Synthetic/Software Defined Instrumentation technology, contrasting it with the classical instrumentation paradigm, as fuel for the panel discussion. Each panelist will then present / provide a "position statement" of their view on state of the art and application spaces the subject technology today, as well as their future prognosis for this innovative technology. Panelist will then be prompted by the moderator as a group to collectively discuss and debate their views on current applications, challenges, and the future course of action they envision for Synthetic/Software Defined Instrumentation technology. The moderator will then query the panel of "Frequently Asked Questions" (FAQs) often posed by new adopters as well as instrumentation traditionalists. During the course of the panel session, the moderator will also prompt and encourage audience interaction with the panel members.

Panelists:

Wade Lowdermilk, *CTO, RADX Systems, USA*

Dave Carey, Ph.D, *Associate Professor of Electrical Engineering, Wilkes University, USA*

Sean Thompson, *A/D Platform Manager, National Instruments, USA*

Jeff Murrill, *Manager ATE Systems Engineering, ATS Systems, Northrop Grumman Corporation, USA*

Wednesday, 18 September

Executive Plenary Panel: Automatic Testing for the Next Decade - Keeping Pace with the New Military
8:00 AM - 10:00 AM
Room: Schaumburg East
Moderator: Michael T. Ellis (Northrop Grumman Corporation, USA)

This year’s conference theme is "ATS Innovation in the Era of Challenging Budgets”. Nowhere is this challenge more obvious that in the Sequestration budget cuts that have forced industry and the military to focus on the ways in which the weapons and weapon's support must change. The mantra of "Doing More with Less" has been with us for decades, but the forced austerity measures of recent times moves the phrase from mantra to mandate. Where should our test industry efforts be focused? How are the needs and the market changing? How can we, as partners with our warfighters, become an integral part of the solution? This panel of industry leaders will explore these questions and offer their vision of the new tomorrow. Following presentations from the panel, attendees are invited to offer their thoughts and questions as we begin another week of sharing concepts, ideas and discussions that will help guide us and our military counterpart through the challenges of the next decade.

“Introduction: The Past as Prolog – Where Have We Been; How Did we Get Here”
Michael Ellis, *Northrop Grumman Corporation*

“Sequestration and ATE Standardization – The Perfect Storm”
David J. Salisbury, *Director, CINS Business Development, Northrop Grumman Corporation*

"Bridging the Armament Test Gap"
Steve Sargeant, *Major General, USAF (Ret.),Chief Executive Officer - Marvin Test Solutions, Inc., Vice President, Strategic Development - The Marvin Group*

"TPS Reuse: A Key Contributor to ATS Affordability"
Chris Clendenin, *Director-Support Equipment Systems & Services, Boeing Defense, Space and Security*

“Public/Private Partnership: Win-Win for the Government and Industry”
Anthony J. Minei, *Deputy Director, Enterprise Test Solutions, Lockheed Martin Training and Logistics*

“Mission Critical Test Systems: What Defense & Commercial Test Can Learn From Each Other”
Eric Starkloff, *Senior Vice President, Product Marketing, National Instruments*

Wednesday, 18 September

ATE Techniques & Applications 1

SESSION A4
10:30 AM - 12:00 PM
Room: Schaumburg G
Session Chair: Dean Matsuura (Teradyne Inc., USA)

Simplify ATE Development and Measurements
Kai-Nian Cheah (Agilent Technologies, Inc., Malaysia)

Using Cloud Computing to Enhance Automatic Test Equipment Testing and Maintenance Capabilities
Dale Reitze (Northrop Grumman Corporation, USA)

LabVIEW based control software for Finger Force Sensor Instrumentation Design
Jose Agraz (University of California Los Angeles, USA)
Robert Pozos (San Diego State University, USA)

Test Techniques

SESSION B4
10:30 AM - 12:00 PM
Room: Schaumburg F
Session Chair: Patrick W Kalgren (Sikorsky Aircraft Corporation, USA)

Using Clifford Algebra to Position a Test Fixture
Nathan Waivio (Northrop Grumman Corporation, USA)

Bus Testing in a Modern Era
Chris Gorringe (Cassidian Test Engineering Services Ltd., United Kingdom)

Verifying Fibre Channel FC-AV ULP Functionality in a UUT
Matthew Dube (Teradyne, Inc., USA)

Wednesday, 18 September

Panel: Status and Outlook of Modular Instrumentation in the T&M Industry

SESSION C4
10:30 AM - 12:00 PM
Room: Schaumburg E
Moderator: Bob Helsel (VXIbus Consortium, PXI Systems Alliance, and AXIe Consortium, USA)

Has modular instrumentation become the defacto standard of automated test?

What is the status and outlook for VXI, PXI, LXI, and AXIe instrumentation? In what applications?

What does this mean for Mil/Aero applications in particular?

Four industry experts will give brief presentations on these topics followed by an interactive panel discussion.

Panelists:

Von Campbell, *Chairman of the Board, AXIe Consortium; Platform Components R&D Manager, Software and Modular Solutions Division, Agilent Technologies, USA*

Larry Desjardin, *President, Modular Methods & former Chairman of the Board for the AXIe Consortium, USA*

Tom Sarfi, *President, VXIbus Consortium; VP Marketing and Business Dept., VTI Instruments Corp., USA*

Luke Schreier, *Senior Group Manager for Automated Test Product Marketing, National Instruments, USA*

Steve Schink, *President, LXI Consortium; Program Manager, Agilent Technologies, USA*

Wednesday, 18 September

ATE Techniques & Applications 2

SESSION A5
1:30 PM - 3:00 PM
Room: Schaumburg G
Session Chair: Jeff Murrill (Northrop Grumman Corporation, USA)

AXIe Local Bus Architecture Delivers Unprecedented Bus Speed and Flexibility
Larry Desjardin (Modular Methods LLC, USA)
Lauri Viitas (Guzik Test and Measurement, USA)

What are we able to do with Test Data or Using LabVIEW to Hone in on Actual Cause of Failures
Larry V. Kirkland (WesTest Engineering Corp., USA)

Taming Complexity While Gaining Efficiency: Requirements for the Next Generation of Test Automation Tools
Abhijit Bansal (dSPACE Inc., USA)
Mahendra Muli (dSPACE Inc., USA)
Kunal Patil (dSPACE Inc., USA)

Test Software Techniques

SESSION B5
1:30 PM - 3:00 PM
Room: Schaumburg F
Session Chair: Ion A. Neag (Reston Software, LLC, USA)

Test Scripting - An Alternative Approach to Real-Time Instrument Control
Yonet A. Eracar (Teradyne Inc., USA)
Michael F. McGoldrick (Teradyne Inc., USA)

High Performance Software with Self-Healing and Self-Naming Properties
William J. Headrick (Lockheed Martin, USA)

Model-Based Testing for Execution Algorithms in the Simulation of Cyber-Physical Systems
Justyna Zander (Gdansk University of Technology, HumanoidWay, Poland, USA)

TECHNICAL SESSIONS

Wednesday, 18 September

Panel: Reduce Costs and Future-Proof Your Systems Using IVI and LXI Standards
SESSION C5 & C6
1:30 PM - 5:00 PM
Room: Schaumburg E
Moderator: Bob Stasonis (Pickering Interfaces, USA)

Panelists:

IVI Instrument Driver Fundamentals Course
Joseph Mueller, *Agilent Technologies, USA*

LXI in Gas Turbine Testing: A Case Study
Tom Sarfi, *VTI Instruments, USA*

LXI in Satellite System Testing
Jochen Wolle, *Rohde-Schwarz, Singapore*

Using LXI to simplify signal management at CERN
Noman Hussain, *Pickering Interfaces, United Kingdom*

Assisting Users with Configuring LXI Devices
Steve Schink, *Agilent Technologies and Conrad Proft, Proft inFocus, USA*

ATE Techniques & Applications 3
SESSION A6
3:30 PM - 5:00 PM
Room: Schaumburg G
Session Chair: Kevin Leduc (EADS North America Test and Services, USA)

ATS Redundant design in support of system & mission sustainability
Larry N. Wilson (National Instruments, USA)
Byron Radle (National Instruments, USA)
Michael N. Granieri (National Instruments, USA)

Standardize on Common Test Hardware with a Flexible Switching Matrix
Jake Harnack (National Instruments, USA)
Brandon Brice (National Instruments, USA)

Hybrid VXI/PXI/LXI Test System Using (MIPSS) IEEE-P1693 Standard
Michael Stora (System Interconnect Technologies, USA)
Steve Mann (BCO, Inc., USA)
Rob Spinner (Advanced Test Technologies, Inc., USA)

Recommendations and Best Practices for creating reusable Test Signal Framework definitions
Chris Gorringe (Cassidian Test Engineering Services Ltd., United Kingdom)
Malcolm Brown (UK MoD, United Kingdom)

Wednesday, 18 September

Design for Testability

SESSION B6
3:30 PM - 5:00 PM
Room: Schaumburg F
Session Chair: Michelle L Harris (Lockheed Martin Simulation, Training, and Support, USA)

Considerations in the Design of a Boundary Scan Runtime Library
Terry Borroz (Teradyne, Inc., USA)

How Much Value Can Testability Add to a System?
Louis Y. Ungar (Advanced Test Engineering (A.T.E.) Solutions, Inc., USA)

Testability verification based on sequential probability ratio test method
Wang Chao (National University of Defense Technology, P.R. China)
Qiu Jing (National University of Defense Technology, P.R. China)
Liu Guan-jun (National University of Defense Technology, P.R. China)
Zhang Yong (National University of Defense Technology, P.R. China)
Zhao Chen-xu (National University of Defense Technology, P.R. China)

A New Testability Model for Better Design and Lower Cost in Electronic Equipment Scheme Design Phase
PengFei Dai (Tsinghua University, P.R. China)
Shiyuan Yang (Tsinghua University, P.R. China)
Jinxia Jiao (Tsinghua University, P.R. China)

Thursday, 19 September

ATE Standards
SESSION A7
9:00 AM - 10:30 AM
Room: Schaumburg G
Session Chair: Louis Y. Ungar (A.T.E. Solutions, Inc., USA)

Reducing Test Program Costs Through ATML-based Requirements Conversion and Code Generation
Lars Lindstrom (National Instruments, USA)
Ion Neag (Reston Software, USA)

Test Program Transportability Using a Common ATE Framework
Steven A. Wegener (Boeing, USA)
Scott Hathaway (Boeing, USA)
Nathan Sander (Boeing, USA)

Architectural considerations for implementation of the ATML standards in an Open Systems Architecture Runtime environment (OSA-RTS) using a graphical environment
Chris Gorringe (Cassidian Test Engineering Services, United Kingdom)
Anand Jain (National Instruments, USA)

Next Generation ATE Software
Richard Hooper (AAI Corporation, USA)

TPS Development
SESSION B7
9:00 AM - 10:30 AM
Room: Schaumburg F
Session Chair: Michael Rutledge (IEEE & EADS North America Test and Services, USA)

ATE Hardware Independent TPS Development Using A Reconfigurable Test Executive
Zafer Savas (ASELSAN Inc., Turkey)
Muharrem Arik (ASELSAN Inc., Turkey)

TPS Solutions for Aircraft Controller System LRIs in Conjunction with LM-STAR®
Steven J. O'Donnell (Lockheed Martin, USA)
Paolo Anzile (Selex ES, Italy)

Research on Technology of ATS Test Program Auto Generating Driven by Test Requirement
Meng Chen (Shijiazhuang Mechanical Engineering College, P.R. China)
Wang Cheng (Shijiazhuang Mechanical Engineering College, P.R. China)
Yang Sen (Shijiazhuang Mechanical Engineering College, P.R. China)

TECHNICAL SESSIONS

Thursday, 19 September

Diagnostics & Prognostics 1

SESSION C7
9:00 AM - 10:30 AM
Room: Schaumburg E
Session Chair: John W. Sheppard (Montana State University, USA)

Diagnostic Bayesian Networks with Fuzzy Evidence
Nicholas Ryhajlo (Montana State University, USA)
Liessman Sturlaugson (Montana State University, USA)
John W. Sheppard (Montana State University, USA)

Multi-Auto Associative Neural network based Sensor Validation and Estimation for Aero-Engine
Brijeshkumar Shah (CSIR-National Aerospace Laboratories, India)
Sarvajith Manjunath (CSIR-National Aerospace Laboratories, India)
Balaji Sankar (CSIR-National Aerospace Laboratories, India)
Thennavarajan Subramanian (CSIR-National Aerospace Laboratories, India)

Abnormalities Ensuing from Back-Tracing and Probe Selection or What Can We Do to Mitigate Diagnostic Problems
Larry V. Kirkland (WesTest Engineering, USA)

ATE Methods

SESSION A8
10:45 AM - 12:15 PM
Room: Schaumburg G
Session Chair: Michael J Dewey (Marvin Test Solutions, USA)

Enabling Communication between ATLAS Environment with an Integrated Subsystem
Alan Kin (Teradyne, Inc., USA)

Leveraging COTS Test Automation Tools Across the Product Lifecycle
Jeff Gray (CertTech, LLC, USA)

Experiences in Replacing Obsolete Spectrum Analyser as part of an ATE uplift program
Chris Gorringe (Cassidian Test Engineering Services Ltd., United Kingdom)

Instrument, Hardware and Software Simulation in a Test System
Ron Yazma (Marvin Test Solutions, USA)

Thursday, 19 September

Test Instrumentation
SESSION B8
10:45 AM - 12:15 PM
Room: Schaumburg F
Session Chair: John A Rosenwald, Jr (AAI Corporation, USA)

Data Compression Methods to Stream Highest Bandwidth Radar Pulses
Michael May (Agilent Technologies, Inc., Germany)

Calibration and Maintenance of Modular Instrument Measurement Systems
Paul Packebush (National Instruments, USA)

Digitizer-based Phase Coherent Measurements for Multi-antenna Phased Array Applications
Alex Dickson (Agilent Technologies, Inc., USA)

Diagnostics & Prognostics 2
SESSION C8
10:45 AM - 12:15 PM
Room: Schaumburg E
Session Chair: Timothy J Wilmering (Boeing, USA)

Using Big Data and Predictive Machine Learning in Aerospace Test Environments
Tom Armes (IntraStage, USA)
Mark Refern (UTC, USA)

Implementing AI-ESTATE with Prognostic Extensions in Java
Liessman Sturlaugson (Montana State University, USA)
Nathan Fortier (Montana State University, USA)
Patrick Donnelly (Montana State University, USA)
John W. Sheppard (Montana State University, USA)

Implementation of Prognostic Methodologies to Cryogenic Propellant Loading Testbed
Chetan S. Kulkarni (SGT Inc. & NASA Ames Research Center, USA)
Matthew Daigle (NASA Ames Research Center, USA)
Kai Goebel (NASA Ames Research Center, USA)